IN THE CLAIMS

CLEAN VERSION - Please amend claims 15, 16 as follows:

1. (Original) A process for fabricating a field-effect semiconductor memory device comprising the steps of:

(a) providing an apparatus including: (i) a silicon substrate; (ii) a first member disposed over said substrate, and said member having at least a first region and a second region; (iii) a first insulator dielectric layer having a first thickness disposed over said first member; (iv) a first conducting layer disposed on said first region of said member and in contact with said first insulator, wherein said first conductive layer having sidewalls including a first sidewall that is disposed over and insulated from said member;

(b) growing a first thermal oxide dielectric layer by oxidation of at least said first sidewall of said first conductive layer to a second thickness to form a thermally-grown portion of an insulation-spacer, wherein said first thermal oxide is disposed over said first member and in contact with said first insulator;

(c) depositing a third dielectric layer including tetramethylsilane (TMS) to a third thickness to be in contact with said first thermal oxide along said first side wall of said first conducting layer to form a deposited portion of said insulation-spacer; and

(d) forming a second conductive layer to be disposed over said second region of said member and along said first sidewall said first conductive layer in a manner to be insulated therefrom, and said second conductive layer is also formed to be in contact with said insulation-spacer including at the location that is opposite said first sidewall of said first conductive layer and in contact with said third dielectric layer.

2. (Original) The process as defined in claim 1, wherein growing said first thermal oxide in step (b) is performed in a manner that retains said first thickness of said first insulator layer substantially unchanged.

3. (Original) The process as defined in claim 1, wherein said first thermal oxide in step (b) is grown to a second thickness and said third dielectric layer of step (c) is a deposited tetramethylsilane (TMS) based silicon dioxide that is formed to have a third thickness that is thicker than said second thickness of said thermal oxide.

4. (Original) The process as defined in claim 1, wherein dielectric constant of said first thermal oxide dielectric layer is higher than the dielectric constant of said third dielectric layer.

5. (Original) The process as defined in claim 1, wherein at least a portion of said member is formed of conductive silicon and at least a portion of said first conductive layer is formed of conductive silicon and at least a portion of said second conductive layer is formed of conductive silicon.

6. (Original) The process as defined in claim 1, wherein said first member is the insulated floating gate, said first conductive layer is the control gate and said second conductive layer is the erase line respectively of an electrically programmable non-volatile memory transistor.

7. (Original) A process for fabricating a field-effect semiconductor memory device comprising the steps of:

(a) providing an apparatus including: (i) a silicon substrate; (ii) a first member disposed over said substrate, and said member having at least a first region and a second region; (iii) a first insulator dielectric layer having a first thickness disposed over said first member; (iv) a first conducting layer disposed on said first region of said member and in contact with said first insulator, wherein said first conductive layer having sidewalls including a first sidewall that is disposed over and insulated from said member;

(b) growing a first thermal oxide dielectric layer by oxidation of at least said first sidewall of said first conductive layer to a second thickness to form a thermally-grown portion of an insulation-spacer, wherein said first thermal oxide that is disposed over said first member and in contact with said first insulator;

(c) depositing a third dielectric layer including tetramethylsilane (TMS) to a third thickness to be in contact with said first thermal oxide along said first side wall of said first conducting layer to form a deposited portion of said insulation-spacer; and

(d) forming a second conductive layer to be disposed over said second region of said member and along said first sidewall said first conductive layer in a manner to be insulated therefrom, and said second conductive layer is also formed to be in contact with said insulation-spacer including at the location that is opposite said first sidewall of said first conductive layer and in contact with said third dielectric layer; thereby said first member is the insulated floating gate, said first conductive layer is the control gate and said second conductive layer is the erase line respectively of an electrically programmable non-volatile memory transistor.

8. (Original) The process as defined in claim 7, wherein growing said first thermal oxide in step (b) is performed in a manner that retains said first thickness of said first insulator layer substantially unchanged.

9. (Original) The process as defined in claim 7, wherein said first thermal oxide

in step (b) is grown to a second thickness and said third dielectric layer of step (c) is a deposited tetramethylsilane (TMS) based silicon dioxide that is formed to have a third thickness that is thicker than said second thickness of said thermal oxide.

10. (Original) The process as defined in claim 7, wherein dielectric constant of said first thermal oxide dielectric layer is higher than the dielectric constant of said third dielectric layer.

11. (Original) The process as defined in claim 7, wherein at least a portion of said member is formed of conductive silicon and at least a portion of said first conductive layer is formed of conductive silicon and at least a portion of said second conductive layer is formed of conductive silicon.

12. (Original) The process as defined in claim 9 wherein said formation of said tetramethylsilane (TMS) oxide is carried out at a temperature of less than 260 degrees centigrade.

13. (Original) The process as defined in claim 7 wherein said first thermal oxide dielectric layer is under 150 angstroms thick.

14. (Original) The process of claim 7 wherein said location where said second conductive layer contacts said third dielectric layer is a surface that is flatter than the side wall of said first conductive layer.

15. (Amended) A process for forming a semiconductor memory cells array wherein each cell has a transistor with a gate and said array having at least two adjacent word lines and at least three adjacent columns of memory cells in order to obtain reduced capacitance between word lines comprising:

forming said adjacent word lines from conductive material so that each of said adjacent word lines is directly connected to said gates of adjacent memory cells of said three adjacent columns and so that each word line has side walls;

forming a first oxide layer that has a first dielectric constant to a first thickness and to be in contact with said adjacent word lines and to be disposed between said adjacent word lines;

forming a second oxide layer including tetramethylsilane (TMS) based silicon dioxide having a second dielectric constant that is lower than said first dielectric constant to a second thickness and to be in contact with said first silicon dioxide and so that said TMS based silicon dioxide is also disposed between the side walls of said adjacent word lines.

16. (Deleted) The process as defined in claim 15, wherein the dielectric constant of said first oxide dielectric layer is higher than the dielectric constant of said TMS oxide dielectric layer.

17. (Unchanged) The process as defined in claim 15, wherein said the second thickness of said TMS based oxide is thicker than the first thickness of said first oxide layer.